IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	09/826693	**Docket Number**	MIPS.0172-00-US
Filed	04/04/01	**Group Art Unit**	2185
Examiner	REGINALD G. BRAGDON	**Customer No.**	23669
Application Title	SYSTEM AND METHOD FOR DATE CACHE BYPASSING IN A STREAM PROCESSING UNIT FOR A MULTI-STREAMING PROCESSOR		
First Named Inventor	MARIO D. NEMIROVSKY		

FACSIMILE COVER SHEET

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To: **Commissioner for Patents - Central Fax Number**
Fax Number: **571-273-8300**

From: **HUFFMAN PATENT GROUP, LLC**
Fax Number: **(661) 460-1986**

Pages: **35 (including this cover sheet)**

Dear Sir:

Please accept the attached correspondence for the above-identified matter. I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

/Richard K. Huffman/

By: _____

RICHARD K. HUFFMAN, P.E.
Registration No. 41,082
Tel: (719) 575-9998

02/01/2006

Date: _____

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LETTER TO EXAMINER

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VIA FACSIMILE: 571-273-8300

Mail Stop **AMENDMENT**
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In the Office Action mailed 01/25/2006, the Examiner noted that citation AP, "Kessler et al.," from the Information Disclosure Statement submitted on 04/21/2005 was not considered because the copy of the document was not legible. The undersigned can only speculate that an illegible copy of the document was produced within the PTO. Accordingly, another copy of that portion of the submittal is attached hereto.

In addition, the undersigned notes that citation AG, "ESA/390 Principles of Operation," from the same Information Disclosure Statement, was not signed off by the Examiner. Perhaps the copy of that portion of the submittal was rendered illegible during copying as well. Accordingly, another copy of citation AG is provided herewith and follows of citation AP.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

/Richard K. Huffman/

By _____

RICHARD K. HUFFMAN
Registration No. 41,082
(719) 575-9998

02/01/2006

Date: _____

COMPAQ
The Alpha 21264 Microprocessor:
Out-of-Order Execution at 600 Mhz
R. E. Kessler
COMPAQ Computer Corporation
Shrewsbury, MA
AP

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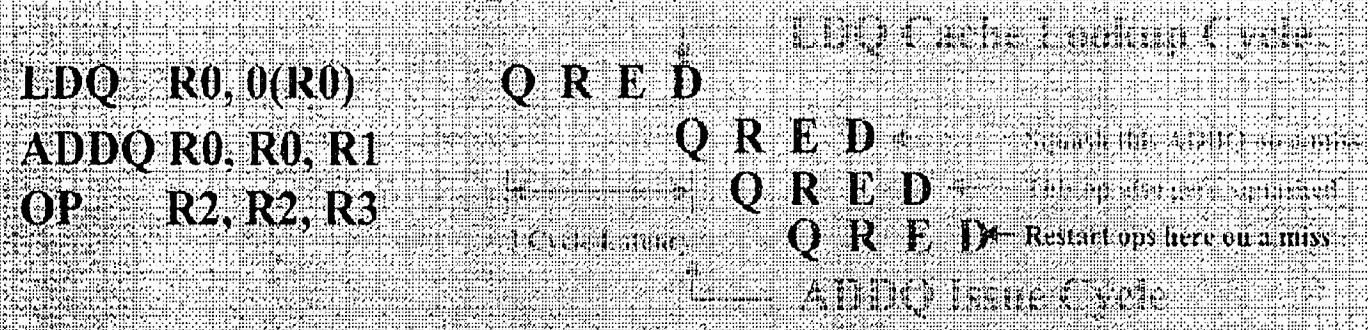
2/1/2006 4:01 PM FROM: 661-460-1986 Huffman Patent Group, LLC TO: 1-571-273-8300 PAGE: 004 OF 035

Low-latency Speculative Issue of Integer Load Data Consumers (Predict Hit)



- **When predicting a load hit:**
  - The ADDQ issues (speculatively) after 3 cycles
  - Best performance if the load actually hits (matching the prediction)
  - The ADDQ issues before the load hit/miss calculation is known
- **If the LDQ misses when predicted to hit:**
  - Squash two cycles (replay the ADDQ and its consumers)
  - Force a "mini-replay" (direct from the issue queue)

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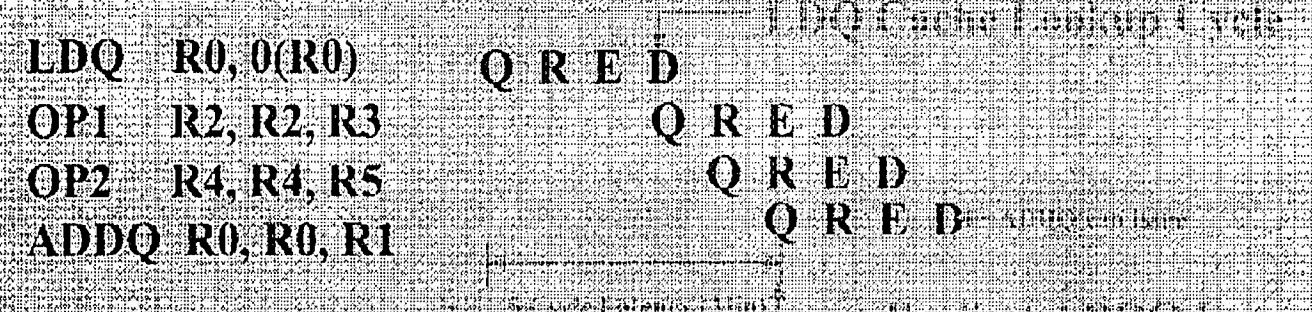
COMPAQ

Low-latency Speculative Issue of Integer Load Data Consumers (Predict Miss)



- **When predicting a load miss:**
  - The minimum load latency is 5 cycles (more on a miss)
  - There are no squashes
  - Best performance if the load actually misses (as predicted)
- **The hit/miss predictor:**
  - MSB of 4-bit counter (hits increment by 1, misses decrement by 2)

Title: ESA/390 Principles of Operation
Document Number: SA22-7201-01
Build Date: 09/23/93 08:36:13 Build Version: 1.2
Book Path: /home/webapps/epubs/ludocs/book/dz9ar001.boo

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7.5.36 LOAD ADDRESS EXTENDED
7.5.37 LOAD AND TEST
7.5.38 LOAD COMPLEMENT

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7.5.39 LOAD HALFWORD
7.5.40 LOAD MULTIPLE
7.5.41 LOAD NEGATIVE
7.5.42 LOAD POSITIVE
7.5.43 MONITOR CALL
7.5.44 MOVE
7.5.45 MOVE INVERSE
7.5.46 MOVE LONG
7.5.47 MOVE NUMERICS
7.5.48 MOVE PAGE (Facility 1)
7.5.49 MOVE STRING
7.5.50 MOVE WITH OFFSET
7.5.51 MOVE ZONES
7.5.52 MULTIPLY
7.5.53 MULTIPLY HALFWORD
7.5.54 OR
7.5.55 PACK
7.5.56 SEARCH STRING
7.5.57 SET ACCESS
7.5.58 SET PROGRAM MASK
7.5.59 SHIFT LEFT DOUBLE
7.5.60 SHIFT LEFT DOUBLE LOGICAL
7.5.61 SHIFT LEFT SINGLE
7.5.62 SHIFT LEFT SINGLE LOGICAL
7.5.63 SHIFT RIGHT DOUBLE
7.5.64 SHIFT RIGHT DOUBLE LOGICAL
7.5.65 SHIFT RIGHT SINGLE
7.5.66 SHIFT RIGHT SINGLE LOGICAL
7.5.67 STORE
7.5.68 STORE ACCESS MULTIPLE
7.5.69 STORE CHARACTER
7.5.70 STORE CHARACTERS UNDER MASK
7.5.71 STORE CLOCK
7.5.72 STORE HALFWORD
7.5.73 STORE MULTIPLE
7.5.74 SUBTRACT
7.5.75 SUBTRACT HALFWORD
7.5.76 SUBTRACT LOGICAL
7.5.77 SUPERVISOR CALL
7.5.78 TEST AND SET
7.5.79 TEST UNDER MASK
7.5.80 TRANSLATE
7.5.81 TRANSLATE AND TEST
7.5.82 UNPACK
7.5.83 UPDATE TREE

8.0 **Chapter 8. Decimal Instructions**

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8.1 Decimal-Number Formats
8.1.1 Zoned Format
8.1.2 Packed Format
8.1.3 Decimal Codes
8.2 Decimal Operations
8.2.1 Decimal Arithmetic Instructions
8.2.2 Editing Instructions
8.2.3 Execution of Decimal Instructions
8.2.4 Other Instructions for Decimal Operands
8.3 Instructions
8.3.1 ADD DECIMAL
8.3.2 COMPARE DECIMAL
8.3.3 DIVIDE DECIMAL
8.3.4 EDIT
8.3.5 EDIT AND MARK
8.3.6 MULTIPLY DECIMAL
8.3.7 SHIFT AND ROUND DECIMAL
8.3.8 SUBTRACT DECIMAL
8.3.9 ZERO AND ADD

9.0 Chapter 9. Floating-Point Instructions
9.1 Floating-Point Number Representation
9.2 Normalization
9.3 Floating-Point-Data Format
9.4 Instructions
9.4.1 ADD NORMALIZED
9.4.2 ADD UNNORMALIZED
9.4.3 COMPARE
9.4.4 DIVIDE
9.4.5 HALVE
9.4.6 LOAD
9.4.7 LOAD AND TEST
9.4.8 LOAD COMPLEMENT
9.4.9 LOAD NEGATIVE
9.4.10 LOAD POSITIVE
9.4.11 LOAD ROUNDED
9.4.12 MULTIPLY
9.4.13 SQUARE ROOT
9.4.14 STORE
9.4.15 SUBTRACT NORMALIZED
9.4.16 SUBTRACT UNNORMALIZED

10.0 Chapter 10. Control Instructions
10.1 BRANCH AND STACK
10.2 DIAGNOSE
10.3 EXTRACT PRIMARY ASN
10.4 EXTRACT SECONDARY ASN

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10.5 EXTRACT STACKED REGISTERS
10.6 EXTRACT STACKED STATE
10.7 INSERT ADDRESS SPACE CONTROL
10.8 INSERT PSW KEY
10.9 INSERT STORAGE KEY EXTENDED
10.10 INSERT VIRTUAL STORAGE KEY
10.11 INVALIDATE PAGE TABLE ENTRY
10.12 LOAD ADDRESS SPACE PARAMETERS
10.13 LOAD CONTROL
10.14 LOAD PSW
10.15 LOAD REAL ADDRESS
10.16 LOAD USING REAL ADDRESS
10.17 MODIFY STACKED STATE
10.18 MOVE PAGE (Facility 2)
10.19 MOVE TO PRIMARY
10.20 MOVE TO SECONDARY
10.21 MOVE WITH DESTINATION KEY
10.22 MOVE WITH KEY
10.23 MOVE WITH SOURCE KEY
10.24 PROGRAM CALL
10.25 PROGRAM RETURN
10.26 PROGRAM TRANSFER
10.27 PURGE ALB
10.28 PURGE TLB
10.29 RESET REFERENCE BIT EXTENDED
10.30 SET ADDRESS SPACE CONTROL
10.31 SET ADDRESS SPACE CONTROL FAST
10.32 SET CLOCK
10.33 SET CLOCK COMPARATOR
10.34 SET CPU TIMER
10.35 SET PREFIX
10.36 SET PSW KEY FROM ADDRESS
10.37 SET SECONDARY ASN
10.38 SET STORAGE KEY EXTENDED
10.39 SET SYSTEM MASK
10.40 SIGNAL PROCESSOR
10.41 STORE CLOCK COMPARATOR
10.42 STORE CONTROL
10.43 STORE CPU ADDRESS
10.44 STORE CPU ID
10.45 STORE CPU TIMER
10.46 STORE PREFIX
10.47 STORE THEN AND SYSTEM MASK
10.48 STORE THEN OR SYSTEM MASK
10.49 STORE USING REAL ADDRESS
10.50 TEST ACCESS
10.51 TEST BLOCK

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10.52 TEST PROTECTION
10.53 TRACE

11.0 **Chapter 11. Machine-Check Handling**
11.1 **Machine-Check Detection**
11.2 **Correction of Machine Malfunctions**
11.2.1 Error Checking and Correction
11.2.2 CPU Retry
11.2.2.1 Effects of CPU Retry
11.2.2.2 Checkpoint Synchronization
11.2.2.3 Handling of Machine Checks during Checkpoint Synchronization
11.2.2.4 Checkpoint-Synchronization Operations
11.2.2.5 Checkpoint-Synchronization Action
11.2.3 Channel-Subsystem Recovery
11.2.4 Unit Deletion
11.3 **Handling of Machine Checks**
11.3.1 Validation
11.3.2 Invalid CBC in Storage
11.3.2.1 Programmed Validation of Storage
11.3.3 Invalid CBC in Storage Keys
11.3.4 Invalid CBC in Registers
11.4 **Check-Stop State**
11.4.1 System Check Stop
11.5 **Machine-Check Interruption**
11.5.1 Exigent Conditions
11.5.2 Repressible Conditions
11.5.3 Interruption Action
11.5.4 Point of Interruption
11.6 **Machine-Check-Interruption Code**
11.6.1 Subclass
11.6.1.1 System Damage
11.6.1.2 Instruction-Processing Damage
11.6.1.3 System Recovery
11.6.1.4 Timing-Facility Damage
11.6.1.5 External Damage
11.6.1.6 Vector-Facility Failure
11.6.1.7 Degradation
11.6.1.8 Warning
11.6.1.9 Channel Report Pending
11.6.1.10 Service-Processor Damage
11.6.1.11 Channel-Subsystem Damage
11.6.2 Subclass Modifiers
11.6.2.1 Vector-Facility Source
11.6.2.2 Backed Up
11.6.2.3 Delayed Access Exception
11.6.3 Synchronous Machine-Check-Interruption Conditions
11.6.3.1 Processing Backup

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11.6.3.2 Processing Damage
11.6.4 Storage Errors
11.6.4.1 Storage Error Uncorrected
11.6.4.2 Storage Error Corrected
11.6.4.3 Storage-Key Error Uncorrected
11.6.4.4 Storage Degradation
11.6.4.5 Indirect Storage Error
11.6.5 Machine-Check Interruption-Code Validity Bits
11.6.5.1 PSW-MWP Validity
11.6.5.2 PSW Mask and Key Validity
11.6.5.3 PSW Program-Mask and Condition-Code Validity
11.6.5.4 PSW-Instruction-Address Validity
11.6.5.5 Failing-Storage-Address Validity
11.6.5.6 External-Damage-Code Validity
11.6.5.7 Floating-Point-Register Validity
11.6.5.8 General-Register Validity
11.6.5.9 Control-Register Validity
11.6.5.10 Storage Logical Validity
11.6.5.11 Access-Register Validity
11.6.5.12 CPU-Timer Validity
11.6.5.13 Clock-Comparator Validity
11.7 **Machine-Check Extended Interruption Information**
11.7.1 Register-Save Areas
11.7.2 External-Damage Code
11.7.3 Failing-Storage Address
11.8 **Handling of Machine-Check Conditions**
11.8.1 Floating Interruption Conditions
11.8.1.1 Floating Machine-Check-Interruption Conditions
11.8.1.2 Floating I/O Interruptions
11.9 **Machine-Check Masking**
11.9.1 Channel-Report-Pending Subclass Mask
11.9.2 Recovery Subclass Mask
11.9.3 Degradation Subclass Mask
11.9.4 External-Damage Subclass Mask
11.9.5 Warning Subclass Mask
11.10 **Machine-Check Logout**
11.11 **Summary of Machine-Check Masking**

12.0 **Chapter 12. Operator Facilities**
12.1 **Manual Operation**
12.2 **Basic Operator Facilities**
12.2.1 Address-Compare Controls
12.2.2 Alter-and-Display Controls
12.2.3 Architectural-Mode Indicator
12.2.4 Architectural-Mode-Selection Controls
12.2.5 Check-Stop Indicator
12.2.6 IML Controls

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12.2.7 Interrupt Key
12.2.8 Load Indicator
12.2.9 Load-Clear Key
12.2.10 Load-Normal Key
12.2.11 Load-Unit-Address Controls
12.2.12 Manual Indicator
12.2.13 Power Controls
12.2.14 Rate Control
12.2.15 Restart Key
12.2.16 Start Key
12.2.17 Stop Key
12.2.18 Store-Status Key
12.2.19 System-Reset-Clear Key
12.2.20 System-Reset-Normal Key
12.2.21 Test Indicator
12.2.22 TOD-Clock Control
12.2.23 Wait Indicator
12.3 **Multiprocessing Configurations**

13.0 **Chapter 13. I/O Overview**
13.1 **Input/Output (I/O)**
13.2 **The Channel Subsystem**
13.2.1 Subchannels
13.3 **Attachment of Input/Output Devices**
13.3.1 Channel Paths
13.3.2 Control Units
13.3.3 I/O Devices
13.4 **I/O Addressing**
13.4.1 Channel-Path Identifier
13.4.2 Subchannel Number
13.4.3 Device Number
13.4.4 Device Identifier
13.5 **Execution of I/O Operations**
13.5.1 Start-Function Initiation
13.5.2 Path Management
13.5.3 Channel-Program Execution
13.5.4 Conclusion of I/O Operations
13.5.5 I/O Interruptions

14.0 **Chapter 14. I/O Instructions**
14.1 **I/O-Instruction Formats**
14.2 **I/O-Instruction Execution**
14.2.1 Serialization
14.2.2 Operand Access
14.2.3 Condition Code
14.2.4 Program Exceptions
14.3 **Instructions**

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14.3.1 CLEAR SUBCHANNEL
14.3.2 HALT SUBCHANNEL
14.3.3 MODIFY SUBCHANNEL
14.3.4 RESET CHANNEL PATH
14.3.5 RESUME SUBCHANNEL
14.3.6 SET ADDRESS LIMIT
14.3.7 SET CHANNEL MONITOR
14.3.8 START SUBCHANNEL
14.3.9 STORE CHANNEL PATH STATUS
14.3.10 STORE CHANNEL REPORT WORD
14.3.11 STORE SUBCHANNEL
14.3.12 TEST PENDING INTERRUPTION
14.3.13 TEST SUBCHANNEL

15.0 **Chapter 15. Basic I/O Functions**
15.1 **Control of Basic I/O Functions**
15.1.1 Subchannel-Information Block
15.1.1.1 Path-Management-Control Word
15.1.1.2 Subchannel-Status Word
15.1.1.3 Model-Dependent Area
15.1.1.4 Summary of Modifiable Fields
15.2 **Channel-Path Allegiance**
15.2.1 Working Allegiance
15.2.2 Active Allegiance
15.2.3 Dedicated Allegiance
15.2.4 Channel-Path Availability
15.2.5 Control-Unit Type
15.3 **Clear Function**
15.3.1 Clear-Function Path Management
15.3.2 Clear-Function Subchannel Modification
15.3.3 Clear-Function Signaling and Completion
15.4 **Halt Function**
15.4.1 Halt-Function Path Management
15.4.2 Halt-Function Signaling and Completion
15.5 **Start Function and Resume Function**
15.5.1 Start-Function and Resume-Function Path Management
15.6 **Execution of I/O Operations**
15.6.1 Blocking of Data
15.6.2 Operation-Request Block
15.6.3 Channel-Command Word
15.6.4 Command Code
15.6.5 Designation of Storage Area
15.6.6 Chaining
15.6.6.1 Data Chaining
15.6.6.2 Command Chaining
15.6.7 Skipping
15.6.8 Program-Controlled Interruption

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15.6.9 CCW Indirect Data Addressing
15.6.10 Suspension of Channel-Program Execution
15.6.11 Commands and Flags
15.6.12 Branching in Channel Programs
15.6.12.1 Transfer in Channel
15.6.13 Command Retry
15.7 **Concluding I/O Operations during Initiation**
15.8 **Immediate Conclusion of I/O Operations**
15.9 **Concluding I/O Operations During Data Transfer**
15.10 **Channel-Path-Reset Function**
15.10.1 Channel-Path-Reset-Function Signaling
15.10.2 Channel-Path-Reset Function-Completion Signaling

16.0 **Chapter 16. I/O Interruptions**
16.1 **Interruption Conditions**
16.1.1 Intermediate Interruption Condition
16.1.2 Primary Interruption Condition
16.1.3 Secondary Interruption Condition
16.1.4 Alert Interruption Condition
16.2 **Priority of Interruptions**
16.3 **Interruption Action**
16.4 **Interruption-Response Block**
16.5 **Subchannel-Status Word**
16.5.1 Subchannel Key
16.5.2 Suspend Control (S)
16.5.3 Extended-Status-Word Format (L)
16.5.4 Deferred Condition Code (CC)
16.5.5 Format (F)
16.5.6 Prefetch (P)
16.5.7 Initial-Status-Interruption Control (I)
16.5.8 Address-Limit-Checking Control (A)
16.5.9 Suppress-Suspended Interruption (U)
16.5.10 Subchannel-Control Field
16.5.10.1 Zero Condition Code (Z)
16.5.10.2 Extended Control (E)
16.5.10.3 Path Not Operational (N)
16.5.10.4 Function Control (FC)
16.5.10.5 Activity Control (AC)
16.5.10.6 Status Control (SC)
16.5.11 CCW-Address Field
16.5.12 Device-Status Field
16.5.13 Subchannel-Status Field
16.5.13.1 Program-Controlled Interruption
16.5.13.2 Incorrect Length
16.5.13.3 Program Check
16.5.13.4 Protection Check
16.5.13.5 Channel-Data Check

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16.5.13.6 Channel-Control Check
16.5.13.7 Interface-Control Check
16.5.13.8 Chaining Check
16.5.14 Count Field
16.6 **Extended-Status Word**
16.6.1 Extended-Status Format 0
16.6.1.1 Subchannel Logout
16.6.1.2 Extended-Report Word
16.6.1.3 Failing-Storage Address
16.6.2 Extended-Status Format 1
16.6.3 Extended-Status Format 2
16.6.4 Extended-Status Format 3
16.7 **Extended-Control Word**

17.0 **Chapter 17. I/O Support Functions**
17.1 **Channel-Subsystem Monitoring**
17.1.1 Channel-Subsystem Timing
17.1.1.1 Channel-Subsystem Timer
17.1.2 Measurement-Block Update
17.1.2.1 Measurement Block
17.1.2.2 Measurement-Block Origin
17.1.2.3 Measurement-Block Key
17.1.2.4 Measurement-Block Index
17.1.2.5 Measurement-Block-Update Mode
17.1.2.6 Measurement-Block-Update Enable
17.1.2.7 Control-Unit-Queuing Measurement
17.1.2.8 Time-Interval-Measurement Accuracy
17.1.3 Device-Connect-Time Measurement
17.1.3.1 Device-Connect-Time-Measurement Mode
17.1.3.2 Device-Connect-Time-Measurement Enable
17.2 **Signals and Resets**
17.2.1 Signals
17.2.1.1 Halt Signal
17.2.1.2 Clear Signal
17.2.1.3 Reset Signal
17.2.2 Resets
17.2.2.1 Channel-Path Reset
17.2.2.2 I/O-System Reset
17.3 **Externally Initiated Functions**
17.3.1 Initial Program Loading
17.3.2 Reconfiguration of the I/O System
17.4 **Status Verification**
17.5 **Address-Limit Checking**
17.6 **Configuration Alert**
17.7 **Incorrect-Length-Indication Suppression**
17.8 **Concurrent Sense**
17.9 **Channel-Subsystem Recovery**

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17.9.1 Channel Report
17.9.2 Channel-Report Word

A.0 **Appendix A. Number Representation and Instruction-Use Examples**
A.1 **Number Representation**
A.1.1 Binary Integers
A.1.1.1 Signed Binary Integers
A.1.1.2 Unsigned Binary Integers
A.1.2 Decimal Integers
A.1.3 Floating-Point Numbers
A.1.4 Conversion Example
A.2 **Instruction-Use Examples**
A.2.1 Machine Format
A.2.2 Assembler-Language Format
A.2.2.1 Addressing Mode in Examples
A.3 **General Instructions**
A.3.1 ADD HALFWORD (AH)
A.3.2 AND (N, NC, NI, NR)
A.3.2.1 NI Example
A.3.3 Linkage Instructions (BAL, BALR, BAS, BASR, BASSM, BSM)
A.3.3.1 Other BALR and BASR Examples
A.3.4 BRANCH AND STACK (BAKR)
A.3.4.1 BAKR Example 1
A.3.4.2 BAKR Example 2
A.3.4.3 BAKR Example 3
A.3.5 BRANCH ON CONDITION (BC, BCR)
A.3.6 BRANCH ON COUNT (BCT, BCTR)
A.3.7 BRANCH ON INDEX HIGH (BXH)
A.3.7.1 BXH Example 1
A.3.7.2 BXH Example 2
A.3.8 BRANCH ON INDEX LOW OR EQUAL (BXLE)
A.3.8.1 BXLE Example 1
A.3.8.2 BXLE Example 2
A.3.9 COMPARE AND FORM CODEWORD (CFC)
A.3.10 COMPARE HALFWORD (CH)
A.3.11 COMPARE LOGICAL (CL, CLC, CLI, CLR)
A.3.11.1 CLC Example
A.3.11.2 CLI Example
A.3.11.3 CLR Example
A.3.12 COMPARE LOGICAL CHARACTERS UNDER MASK (CLM)
A.3.13 COMPARE LOGICAL LONG (CLCL)
A.3.14 COMPARE LOGICAL STRING (CLST)
A.3.15 CONVERT TO BINARY (CVB)
A.3.16 CONVERT TO DECIMAL (CVD)
A.3.17 DIVIDE (D, DR)
A.3.18 EXCLUSIVE OR (X, XC, XI, XR)
A.3.18.1 XC Example

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A.3.18.2 XI Example
A.3.19 EXECUTE (EX)
A.3.20 INSERT CHARACTERS UNDER MASK (ICM)
A.3.21 LOAD (L, LR)
A.3.22 LOAD ADDRESS (LA)
A.3.23 LOAD HALFWORD (LH)
A.3.24 MOVE (MVC, MVI)
A.3.24.1 MVC Example
A.3.24.2 MVI Example
A.3.25 MOVE INVERSE (MVCIN)
A.3.26 MOVE LONG (MVCL)
A.3.27 MOVE NUMERICS (MVN)
A.3.28 MOVE STRING (MVST)
A.3.29 MOVE WITH OFFSET (MVO)
A.3.30 MOVE ZONES (MVZ)
A.3.31 MULTIPLY (M, MR)
A.3.32 MULTIPLY HALFWORD (MH)
A.3.33 OR (O, OC, OI, OR)
A.3.33.1 OI Example
A.3.34 PACK (PACK)
A.3.35 SEARCH STRING (SRST)
A.3.35.1 SRST Example 1
A.3.35.2 SRST Example 2
A.3.36 SHIFT LEFT DOUBLE (SLDA)
A.3.37 SHIFT LEFT SINGLE (SLA)
A.3.38 STORE CHARACTERS UNDER MASK (STCM)
A.3.39 STORE MULTIPLE (STM)
A.3.40 TEST UNDER MASK (TM)
A.3.41 TRANSLATE (TR)
A.3.42 TRANSLATE AND TEST (TRT)
A.3.43 UNPACK (UNPK)
A.3.44 UPDATE TREE (UPT)
A.4 **Decimal Instructions**
A.4.1 ADD DECIMAL (AP)
A.4.2 COMPARE DECIMAL (CP)
A.4.3 DIVIDE DECIMAL (DP)
A.4.4 EDIT (ED)
A.4.5 EDIT AND MARK (EDMK)
A.4.6 MULTIPLY DECIMAL (MP)
A.4.7 SHIFT AND ROUND DECIMAL (SRP)
A.4.7.1 Decimal Left Shift
A.4.7.2 Decimal Right Shift
A.4.7.3 Decimal Right Shift and Round
A.4.7.4 Multiplying by a Variable Power of 10
A.4.8 ZERO AND ADD (ZAP)
A.5 **Floating-Point Instructions**
A.5.1 ADD NORMALIZED (AD, ADR, AE, AER, AXR)

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A.5.2 ADD UNNORMALIZED (AU, AUR, AW, AWR)
A.5.3 COMPARE (CD, CDR, CE, CER)
A.5.4 DIVIDE (DD, DDR, DE, DER)
A.5.5 HALVE (HDR, HER)
A.5.6 MULTIPLY (MD, MDR, ME, MER, MXD, MXDR, MXR)
A.5.7 Floating-Point-Number Conversion
A.5.7.1 Fixed Point to Floating Point
A.5.7.2 Floating Point to Fixed Point
A.6 **Multiprogramming and Multiprocessing Examples**
A.6.1 Example of a Program Failure Using OR Immediate
A.6.2 Conditional Swapping Instructions (CS, CDS)
A.6.2.1 Setting a Single Bit
A.6.2.2 Updating Counters
A.6.3 Bypassing Post and Wait
A.6.3.1 Bypass Post Routine
A.6.3.2 Bypass Wait Routine
A.6.4 Lock/Unlock
A.6.4.1 Lock/Unlock with LIFO Queuing for Contentions
A.6.4.2 Lock/Unlock with FIFO Queuing for Contentions
A.6.5 Free-Pool Manipulation
A.7 **Sorting Instructions**
A.7.1 Tree Format
A.7.2 Example of Use of Sort Instructions

B.0 **Appendix B. Lists of Instructions**

C.0 **Appendix C. Condition-Code Settings**

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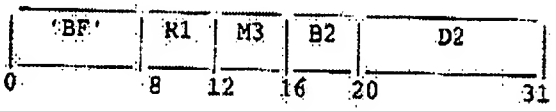
7.5.31 INSERT CHARACTERS UNDER MASK

```
ICM     R1,M3,D2(B2)        [RS]
```



Bytes from contiguous locations beginning at the second-operand address are inserted into general register R1 under control of a mask.

The contents of the M3 field are used as a mask. These four bits, left to right, correspond one for one with the four bytes, left to right, of general register R1. The byte positions corresponding to ones in the mask are filled, left to right, with bytes from successive storage locations beginning at the second-operand address. When the mask is not zero, the length of the second operand is equal to the number of ones in the mask. The bytes in the general register corresponding to zeros in the mask remain unchanged.

The resulting condition code is based on the mask and on the value of the bits inserted. When the mask is zero or when all inserted bits are zeros, the condition code is set to 0. When the inserted bits are not all zeros, the code is set according to the leftmost bit of the storage operand: if this bit is one, the code is set to 1; if this bit is zero, the code is set to 2.

When the mask is not zero, exceptions associated with storage-operand access are recognized only for the number of bytes specified by the mask. When the mask is zero, access exceptions are recognized for one byte at the second-operand address.

Resulting Condition Code:

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0 All inserted bits zeros, or mask bits all zeros
1 Leftmost inserted bit one
2 Leftmost inserted bit zero, and not all inserted bits zeros
3 --

Program Exceptions:

- Access (fetch, operand 2)

Programming Notes:

1. Examples of the use of the INSERT CHARACTERS UNDER MASK instruction are given in Appendix A, "Number Representation and Instruction-Use Examples."

2. The condition code for INSERT CHARACTERS UNDER MASK is defined such that, when the mask is 1111, the instruction causes the same condition code to be set as for LOAD AND TEST. Thus, the instruction may be used as a storage-to-register load-and-test operation.

3. INSERT CHARACTERS UNDER MASK with a mask of 1111 or 0001 performs a function similar to that of a LOAD (L) or INSERT CHARACTER (IC) instruction, respectively, with the exception of the condition-code setting. However, the performance of INSERT CHARACTERS UNDER MASK may be slower.

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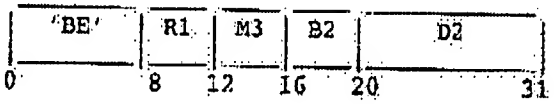
7.5.70 STORE CHARACTERS UNDER MASK

STCM R1,M3,D2(B2) [RS]



Bytes selected from general register R1 under control of a mask are placed at contiguous byte locations beginning at the second-operand address.

The contents of the M3 field are used as a mask. These four bits, left to right, correspond one for one with the four bytes, left to right, of general register R1. The bytes corresponding to ones in the mask are placed in the same order at successive and contiguous storage locations beginning at the second-operand address. When the mask is not zero, the length of the second operand is equal to the number of ones in the mask. The contents of the general register remain unchanged.

When the mask is not zero, exceptions associated with storage-operand accesses are recognized only for the number of bytes specified by the mask.

When the mask is zero, the single byte designated by the second-operand address remains unchanged; however, on some models, the value may be fetched and subsequently stored back unchanged at the same storage location. This update appears to be an interlocked-update reference as observed by other CPUs.

Condition Code: The code remains unchanged.

Program Exceptions:

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- Access (store, operand 2)

Programming Notes:

1. An example of the use of the STORE CHARACTERS UNDER MASK instruction is given in Appendix A, "Number Representation and Instruction-Use Examples."

2. STORE CHARACTERS UNDER MASK with a mask of 0111 may be used to store a three-byte address, for example, in modifying the address in a CCW.

3. STORE CHARACTERS UNDER MASK with a mask of 1111, 0011, or 0001 performs the same function as STORE, STORE HALFWORD, or STORE CHARACTER, respectively. However, on most models, the performance of STORE CHARACTERS UNDER MASK is slower.

4. Using STORE CHARACTERS UNDER MASK with a zero mask should be avoided since this instruction, depending on the model, may perform a fetch and store of the single byte designated by the second-operand address. This reference is not interlocked against accesses by channel programs. In addition, it may cause any of the following to occur for the byte designated by the second-operand address: a PER storage-alteration event may be recognized; access exceptions may be recognized; and, provided no access exceptions exist, the change bit may be set to one. Because the contents of storage remain unchanged, the change bit may or may not be one when a PER storage-alteration event is recognized.

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